

Application No.: 09/801,350

Docket No.: JCLA6643-R4

REMARKS

Appellants appeal the application under 35 U.S.C. 134(a) from Examiner's final rejection of claims 1-4, 13 and 15. The Board affirm the final rejection under 35 U.S.C 6(b). In response, Applicants have amended claim 1, and submit the amendment with a request for continued examination (RCE) under 37 CFR 1.114 to reopen prosecution of the application. In addition, Applicants respectfully traverse the Board Decision and final rejections addressed to claims 1-4, 13 and 15 for at least the reasons set forth below.

Discussion of the claim rejection under 35 USC 102 and 103

In the Decision, the Board states that "we find no basis in the language of claim 1 or in the disclosure in the specification on which to read the disputed language in the narrow sense urged by Appellants. The Board also declines to adopt Appellants' proposed narrow claim interpretation. Therefore, In the Decision, the board broadens the connection relationship of claim 1.

1. Claims 1, 3, 4 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Lin (5,982,601).

Applicants have amended claim 1 above to clarify the connection among terminals of claimed elements. After amended, Applicants believe that claim 1 is not anticipated by the Lin reference.

Applicants respectfully submit that Lin fails to teach or disclose that the first connection

Application No.: 09/801,350

Docket No.: JCLA6643-R4

terminal and the second connection terminal of the SCR circuit are respectively connected to the I/O pad and a ground voltage, and the fourth connection terminal, the fifth connection terminal, and the sixth connection terminal of the anti-latch-up circuit are respectively coupled to the voltage source, the ground voltage, and the third connection terminal of the SCR circuit as recited by the proposed independent claim 1. Instead, Lin substantially discloses that the Three connection terminals of the transient oscillator circuit 61 are respectively connected to the VDD bus or the I/O pad, the SCR circuit and the ground (VSS bus), and the three connection terminals of the SCR circuit are respectively connected to the VDD bus or the I/O pad and the ground (VSS bus) and the transient oscillator circuit 61 (please see FIG. 6A and 9). Therefore, it is clearly evident that Lin substantially fails to teach or disclose the exact connections as claimed in claim 1 of the invention.

Furthermore, the Examiner has misinterpreted that the pad line functions as TWO SEPARATE ELEMENTS; namely, the I/O PAD as well as the VOLTAGE SOURCE. However, the Figure 6A and 9 of Lin, and the related text, very clearly shows that the (first) connection terminal of the SCR circuit and the (fourth) connection terminal of the transient oscillator circuit 61 are respectively connected to the SAME VDD bus or the SAME I/O Pad. Therefore, the Examiner has misinterpreted that the first connection terminal of the SCR circuit of Lin is connected to the I/O pad and the fourth connection terminal of the transient oscillator circuit 61 of Lin is connected to the voltage source or the pad line, which is different from I/O pad.

Because Lin substantially teaches that the connection terminals of BOTH transient oscillator circuit 61 and SCR circuit are connected to the SAME VDD bus or the SAME I/O

Application No.: 09/801,350

Docket No.: JCLA6643-R4

PAD, and therefore one transient circuit is required for each of the VDD bus or the I/O pad. In other words, Lin because fails to teach or disclose that the first connection terminal of the SCR circuit is connected to the I/O pad and the fourth connection terminal of the transient oscillator circuit 61 is connected to the voltage source. Thus, the structure of the ESD protection device of Lin is substantially different compared to the structure of the ESD protection device of the present invention. Accordingly, Lin cannot possibly anticipate the proposed independent claim 1, and therefore the proposed independent claim 1 patentably defines over Lin, and should be allowed.

Also, the claim 3 recites an structure of the SCR circuit (claim 1), and claim 4 recites and structure of the anti-latch-up circuit (claim 1). For at least the same reason as described above, claim 1 patently defines over the Lin reference, claims 3 and 4 also patently defines over the Lin reference.

Claim 13 recites that the anti-latch-up signal can send a voltage signal from the sixth connection terminal to the SCR circuit. Since the circuit structure of claim 1 is clearly different from the Lin reference, claim 13 is thus patently defines over the Lin reference.

In summary, since claims 1, 3, 4 and 13 are not anticipated by the Lin reference, the rejection under 35U.S.C. 102 (b) should be withdrawn and claims 1, 3, 4 and 13 should be allowed.

2. Claims 1, 3-4, 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Quigley (5,781,388) in view of Lin (5,982,601). In addition, claim 15 is rejected under 35

Application No.: 09/801,350

Docket No.: JCLA6643-R4

U.S.C. 103(a) as being unpatentable over Lin.

In response, Applicants have amended claim 1 above to clarify the difference between claim 1 features and the Quigley reference in view of the Lin reference.

Quigley, at Figure 1, substantially teaches or shows that the connection terminals of BOTH voltage divider (17 and 18) and SCR circuit 22 are connected to the SAME I/O PAD.

Quigley, like Lin, at Figure 1, substantially teaches or shows that the connection terminals of BOTH voltage divider (17 and 18) and SCR circuit 22 are connected to the I/O PAD. In other words, Quigley fails to teach or disclose that the first connection terminal of the SCR circuit is connected to the I/O pad and the fourth connection terminal of the transient circuit is connected to the voltage source, instead, Quigley substantially teaches or shows that the connection terminals of BOTH voltage divider (17 and 18) and SCR circuit 22 are connected to the SAME I/O PAD. Therefore one voltage divider (17 and 18) is required for each of the I/O pads.

The Figure 1 of Quigley, and the related text, very clearly shows that the (first) connection terminal of the SCR circuit and the (fourth) connection terminal of the voltage divider are respectively connected to the SAME I/O Pad. Therefore, the Examiner has misinterpreted that the first connection terminal of the SCR circuit of Quigley is connected to the I/O pad and the fourth connection terminal of the voltage divider of Quigley is connected to the voltage source or the pad line, which is different from I/O pad.

In the claimed invention, as clearly recited in claim 1, and also as clearly shown in Figure 4, the first connection terminal (112) of the SCR circuit (104) is connected to "a I/O pad" (100); and the fourth connection terminal (126) of the anti-latch-up circuit (110) is connected to "a

Application No.: 09/801,350

Docket No.: JCLA6643-R4

voltage source" (Vcc). The language "the first connection terminal (112, of the SCR circuit) is connected to a I/O pad" and "fourth connection terminal (126, of the anti-latch-up circuit) is coupled to a voltage source (Vcc)" clearly indicate that the I/O PAD and the VOLTAGE SOURCE are TWO SEPARATE ELEMENTS, and that the first connection terminal of the SCR circuit and the fourth connection terminal of the anti-latch-up circuit are respectively connected to DIFFERENT ELEMENTS, namely, the I/O PAD and the VOLTAGE SOURCE, which is also fully supported by Figure 4.

Thus, the structure of the ESD protection device of Quigley is substantially different compared to the structure of the ESD protection device of the present invention.

Accordingly, the combination of Quigley and Lin, in a manner suggested by the Examiner, cannot possibly render every features of the proposed independent claim 1 obvious in this regard, and therefore the proposed independent claim 1 patently defines over Quigley and Lin and should be allowed.

Also, the remaining claims 3, 4, 13 and 15 depend directly or indirectly from the proposed independent claim 1, and therefore patently define over Quigley and Lin for at least the reasons cited above.

For at least the same reasons discussed above, claim 15 patently defines over Lin, and the rejection should be withdrawn.

3. Claim 2 is rejected under 35 U.S.C 103(a) as being unpatentable over Quigley and Lin and further in view of Ker et al. In addition, claim 2 is rejected under 35 U.S.C. 103(a) as being

Application No.: 09/801,350

Docket No.: JCLA6643-R4

unpatentable over Lin in view of Ker et al (5,754,380)

The disclosures of Quigley and Lin are discussed above. Ker discloses a COMS output buffer with enhanced high ESD protection capability, in which diodes 60 and 70 are serially connected between power lines VDD and VSS to serve as discharge pathways.

However, as discussed above, since Lin, Quigley or Ouigley in view of Lin fails to disclose the claimed circuit structure, even though Lin or Quigley uses the Ker's teachings to insert the diode string between power lines VDD and VSS, the alleged combination still fails to disclose claimed structure as defined in claim 2 of the invention.

As a result, claim 2 does patently defines over Lin in view of Ker, or over Quigley in view of Ker, and the rejection should be withdrawn.

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Application No.: 09/801,350

Docket No.: JCLA6643-R4

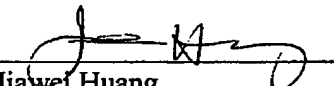
CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-4, 13 and 15 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Date: 7-28-2009

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